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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/749,734 | 12/30/2003 | Yibin Ye | 110350-134110 | 9041 |

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| EXAMINER | |
|---|---|
| LE, THONG QUOC | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2827 | |

DATE MAILED: 08/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/749,734 | YE ET AL. | |
| | Examiner | Art Unit | |
| | Thong Q. Le | 2827 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *29 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-3,11-17 and 21-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,11-17 and 21-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Amendment filed on 07/29/2005 has been entered.

2. Claims 1-3,11-17,21-23 are presented for examination.

### *Specification*

3. The disclosure is objected to because of the following informalities: on page 10 should be changed "**510**" to –"**110**" as shown in Figure 5.

Appropriate correction is required.

### *Claim Objections*

4. Regarding claims 1, 21, line 4, should be changed " second gates" to –second gate--.

### *Response to Arguments*

5. Applicant's arguments filed 07/29/2005 have been fully considered but they are not persuasive.

The Arguments is improper for at least the following reasons:

> In rejecting claim 1, the Examiner cites *van der Wagt*, which discloses two-transistor DRAM cells that include p-channel and n-channel FETs. However, each of the two-transistor DRAM cells that are taught in *van der Wagt* have the p-channel FET as the write device, while the n-channel FET as the read device. *See* figures 2a to 2d, and figure 4 of *van der Wagt*. *Van der Wagt* does not disclose or suggest a two-transistor DRAM cell that includes an NMOS as the write device, and a PMOS as the read device, wherein the storage node is coupled to the gate of the PMOS. For at least these reasons, claim 1 is patentable over *van der Wagt*. Amended independent claim 21 has features similar to those in amended independent claim 1. Therefore, for at least the same reasons that claim 1 is patentable over *van der Wagt*, claim 21 is also patentable over *van der Wagt*.

Since claims 1 and 21 in present application, applicant does not provide an NMOS is defined as the write device, and a PMOS is defined as a read device in claim 1. More specifically, in specification page 8, and figures 3 and 5, **applicant disclosed a PMOS transistor 305 (TW) is a read device, and an PMOS transistor 110 (TR) is a read device in page 8, lines 5-6, lines 9-10**. For these reasons, the applicant's arguments become improperly.

Therefore, the last rejection action is still stand.

### *Claim Rejections - 35 USC § 102*

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-3, 21-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Van der Wagt (U.S. Patent No. 5,953,249).

Regarding claims 1-3, 21-23, Van der Wagt discloses a two-transistor DRAM cell (Figure 4) comprising:

a NMOS device with a first gate (22) ; and a PMOS device with a second gate (20), the PMOS device coupled to the NMOS device; and a storage node (SN) coupled to the second gate (Figure 4, 22), and wherein the storage node is defined the PMOS device and NMOS device, the storage node having a voltage that converges to Vhigh, where Vhigh is greater than Vcc/2 (Figure 5), and NMOS device (22) coupled between

the read bit line (BL) and the read word line (READ WL), a PMOS device coupled to NMOS device so as to define a storage node therebetween (Figure 4, SN), and wherein the IC comprises a CPU, and at least one input/output module coupled to the CPU and memory is coupled to the IC via the communication channel (Column 1, lines 1-27).

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 11-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van der Wagt (U.S. Patent No. 5,953,249), Yoshimoto et al. (U.S. Patent No. 5,010,519) and further in view of Atwood et al. (U.S. Patent No. 6,787,835).

10. Claims 1-3, 21-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoshimoto et al. (U.S. Patent No. 5,010,519).

As described above, and Figure 3 of Yoshimoto et al. disclosed all of elements except a PMOS device is coupled to read bit line and read word line, and an NMOS device is coupled to write bit line. However, Atwood et al. discloses a DRAM cell (Figure 3, MC) can substitute NMOS device is PMOS or PMOS can be NMOS (Column 8, lines 28-39).

In the memory cell of this embodiment, an N-channel device or P-channel device can be used as the storage device, or efforts can be made to adjust the threshold voltage of the device so that the data line to source node capacitance is increased during the write operation. In order to explain the occasions when these cases may be beneficial, a more accurate circuit diagram of the cell is presented in FIG. 8. In an actual semiconductor memories, there will exist a capacitance CW between the write word line WW0 and the storage node NS as well as a capacitance CI between the storage node NS and the intermediate node NI shared by the read transistor QR and the storage transistor QS.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use NMOS or PMOS transistors. Applicant has not disclosed that the position of n-channel or p-channel transistors provide an advantage, is used for particular purpose, or solve a stated problem. For example, in claim 3 of present application, a NMOS device is used to couple between the read bit line and a read word line.

Therefore, it would have been obvious to a person of ordinary skill in this art to modify to use type of transistors to obtain the invention as specified in claim 11.

***Conclusion***

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai V. Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2827

THONG LE
PRIMARY EXAMINER